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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,239	CHOI, JONG-HYUN	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006 and 14 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,10-13,15-24,26,28-33 and 35-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,10-13,15-24,26,28-33 and 35-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20061130*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

After an Advisory Action was mailed with respect to the amendment and replacement sheets previously submitted on Oct 16, 2006 had been reviewed and considered, that amendment and its accompanying replacement sheets had been entered. That amendment and the replacement sheets have accomplished the following:

The replacement sheets overcame the drawing objections described on page 5 of the previous Office Action. Therefore, those objections have been withdrawn.

The amended title overcame its objection, which has now been withdrawn. One of ordinary skill in the art would understand the newly added "with Dual Insulation System" phrasing refers to the thick and thin gate insulations of the MOS transistors cited within the claims.

The amended paragraph, and/or applicant's comments, overcame the objections to the disclosure described on page 6 of the previous Office Action, and those objections have also been withdrawn.

The cancellation of claims 7 and 25 rendered their corresponding objection, and/or rejection, moot.

Amended claims 19 and 29 overcame the objections of claims 19-31 described on page 6 of the previous Office Action. Those claim objections have been withdrawn. However, some previously overlooked concerns were noted, and/or some amended changes created new concerns within the claims.

Amended claims 5-6, 8-10, 15-16, 18, 26, 28-32, and 36-37 overcame most of the rejections of claims 5-13, 15-18, 25-33, and 35-37 under 35 U.S.C. 112 as described on pages 7-8 of the previous Office Action. However, some of those rejections were either not satisfactorily addressed, or the amended change(s) created new concerns, within the claims.

Amended claim 19 overcame the rejections of claims 19-24, and 26 under 35 U.S.C. 102(e), with respect to Wright et al., as described on pages 9-10 of the previous Office Action. Those rejections have been withdrawn because Wright does not clearly show or disclose the fifth MOS transistor controlled by a first input signal including a row address signal and a block selecting signal as now recited within claim 19.

Since the previous Office Action's prior art rejections, and most of the claim rejections under 35 U.S.C. 112, had been overcome, the applicant's representative Linus Park (Reg. No. 45,261) contacted the examiner on Nov 30, 2006 to discuss ways to overcome the remaining, and/or newly created, concerns. This discussion led to the amendment submitted on Dec 14, 2006, which should have theoretically placed the application into condition for allowance.

Transitional After Final Practice

However, when the Dec 14th amendment was carefully reviewed and considered, it was noted that cancelled claims 8-9 did render their rejections moot, and the amended claims overcame most of the known concerns that had been previously identified, but various oversights were also noted, and most importantly, after consulting another examiner with respect to the prior art of record and the claimed limitations, the allowable material identified in the previous Office Action (e.g. with respect to a row address signal) was not deemed to be actually allowable. For example, although the claims cite: 1) one MOS transistor is controlled by a row

address signal (e.g. see claims 1 and 32); 2) the second input signal includes a row address signal (e.g. see claim 10); and 3) the first input signal includes a row address signal and a block selecting signal (e.g. see claim 19), the prior art references showing/disclosing the same type of circuit structure as recited within the claim(s) will also have the capability of receiving such an input signal.

Therefore, the finality of the previous Office Action has now been withdrawn, and the applicant's Amendment after Final submitted on Dec 14, 2006 has been entered. New objections and prior art rejections are described below under their appropriate section, making this action NON-FINAL.

Claim Objections

Claims 1-3, 5-6, 15-16, and 35 are objected to because of the following informalities: Claim 1, line 10 should have "voltage" changed to --circuit-- to correspond to the "first internal circuit" cited on lines 2 and 6. Claim 15, line 2 should have "third" changed to --second--. [Using the applicant's own Fig. 1 as an example, transistors MP1 and MN1 correspond to claim 10's first and second transistors, respectively since these two transistors each have their respective drain directly coupled to power terminal OUT. The drain of third transistor MN2 is coupled to power terminal OUT through second transistor MN1.] Claim 35, lines 1-2 should have both occurrences of "a" changed to --the-- since the third MOS transistor, and its thin gate insulation layer, were previously described in claim 32, lines 8-9. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

After carefully reviewing and reconsidering the active claims, claims 1-3, 5-6, 10-13, 15-18, 28-33, and 35-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 1, "operating at a first voltage higher than a power supply voltage" and "operating at a second voltage lower than the first voltage" cited on respective lines 3 and 4-5 are misleading, and/or confusing, thus requiring clarification. [Using the applicant's own Fig. 1 as an example, first internal circuit/MOS transistor 12/MP1 can be considered as "operating at a first voltage higher than a power supply voltage" in two separate ways: 1) with the source of MP1 coupled to first voltage VPP, the circuit/transistor will operate (i.e. be in conducting and non-conducting states) at that voltage; and 2) with its gate coupled to first voltage VPP, the circuit/transistor will actually be turned off. Therefore, is this the operation the applicant meant? However, since a MOS transistor can be operated in two distinct states (i.e. conducting and non-conducting operations), it is not clear in claim 1 if the first internal circuit/MOS transistor is considered to be operating only when the first voltage is continuously applied (i.e. at the source), when it is being selectively applied (i.e. at the gate), or when the transistor is conducting. Therefore, clarification is requested with respect to what "operating at a first voltage higher than a power supply voltage" actually means within the claim.] Similarly, clarification is requested with respect to what "operating at a second voltage lower than the first voltage" means within claim 1. Claim 6, lines 2-3 "operating at a third voltage higher than the

power supply voltage" also needs clarification. [Using the applicant's Fig. 3 as an example, inverter INV will operate whether a high or low voltage is present at input ND1, wherein high voltage VPP is always coupled to the source of PMOS transistor MP4. For example, if a high voltage is provided at input ND1, MP4 is off and MN8 is on and pulling OUT down to VSS, wherein if a low voltage is provided at input ND1, MP4 is conducting and pulling OUT up to high voltage VPP, while MN8 is off. Therefore, is the operation considered continuous or selective in nature?] The use of "receiving a high voltage" on line 2 of both claim 10 is misleading, and thus confusing. For example, does this imply the terminal receives the high voltage continuously, such as a power supply terminal that is connected to always receive the power supply voltage when the circuit is powered up and in normal operation, or does the power terminal only selectively receive the high voltage? It is believed the power terminal corresponds to node ND1 (of Fig. 3) or OUT (of Fig. 1), wherein high voltage VPP will only be received at this terminal when the first (e.g. PMOS) transistor is conducting. Thus, clarification is requested with respect to what "receiving a high voltage" means in claim 10. For the same type of reasoning as described above with respect to claim 6, "operating at another voltage higher than the power supply voltage" within each of claims 16 and 31 also needs clarification. It is not clear how the plural "row address signals" of claim 28 relate to the singular "row address signal" cited in claim 19. Also; for the same type of reasoning as described above with respect to claim 1, "operating at a first voltage higher than the power supply voltage" and "operating at a second voltage that is lower than the first voltage" on respective lines 3 and 5 of claim 32 need clarification. Dependent claims carry over objection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-6, 10-13, 15-18, 32-33, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardee (reference C cited previously on the PTO-892 of paper number 02092006), in view of Origasa (a reference found during the recent update search). One of ordinary skill in the art would understand that Fig. 1 of Hardee shows a level shifting type device for receiving an input signal alternating between 0V and VCC, and for effectively providing a corresponding output signal that will selectively alternate between 0V and VCCP. The device comprises first internal circuit 12, including first MOS transistor 12, operating at first voltage VCCP higher than power supply voltage VCC of the device (e.g. see column 1, lines 25-28); second internal circuit 16, including second MOS transistor 16, operating at second voltage VCC lower than first voltage VCCP; and restricting means 14, including third MOS transistor 14 with a thin gate insulation layer (i.e. THIN OXIDE) and operating at second voltage VCC, wherein restricting means 14 will restrict a voltage transmitted from first internal circuit 12 to second internal circuit 16 by applying the voltage from first internal circuit 12 to second internal circuit 16 through third MOS transistor 14. Although second MOS transistor 16 is controlled by the input signal alternating between VCC and 0V, this signal is not clearly shown or disclosed as being related to a row address signal in a memory device. However, one of ordinary skill in the art would understand Hardee's device would be capable of operating with a row address signal

as its input signal. Column 1, lines 24-28 of Hardee disclose the device can relate to memory devices which may require the higher voltage, and therefore could be used with a memory device and its related signals. Origasa shows and discloses a memory device in Fig. 2 that utilizes circuit 200, one type of a level shifter, for providing output signal WL that will selectively alternate between Vss and Vwl with respect to an input signal that selectively alternates between Vss and Vcc (e.g. see Figs. 3 and 10). Therefore, it would have been obvious to one of ordinary skill in the art to supply second MOS transistor 16 of Hardee with a row address signal in a memory device, and/or to replace Origasa's level shifting type circuitry 30,300-301 with Hardee's device, wherein second MOS transistor 16 would be controlled by at least one row address signal XAj,XBj through Origasa's logic gate 307, rendering claim 1 obvious. The type of signal applied to Hardee's second MOS transistor would depend on what type of input signal is to be shifted to provide a higher "high" level output. Since first MOS transistor 12 has a thick gate insulation layer (i.e. THICK OXIDE), and second MOS transistor 16 has a thin gate insulation layer (i.e. THIN OXIDE), it would be obvious to one of ordinary skill in the art that the voltage transmitted from first internal circuit 12 to second internal circuit 16 would reduce an electric field applied to the gate insulation layer of second MOS transistor 16 since restricting means 14 functions at a resistance device that provides a voltage drop across it, thus rendering claim 2 obvious. Second voltage VCC is a power supply voltage that would be either an external power supply voltage, or an internal power supply voltage, for the device, and claim 3 is rendered obvious. It would have been obvious to one of ordinary skill in the art to couple an inverter to a connection node between the first and third MOS transistors (i.e. 12 and 14, respectively) of Hardee, wherein the inverter would drive a word line in the memory device, rendering claim 5

obvious. The inverter would provide an inverted version of the output signal from Hardee's circuit, if it was desired, and also provide one means for isolating the word line from Hardee's device. It would be obvious to one of ordinary skill in the art that the inverter include PMOS and NMOS transistors (e.g. see Origasa's inverter 300-301) operating at a third voltage VCCP (of Hardee) or Vwl (of Origasa) higher than power supply voltage VCC, wherein each transistor would have a thick gate insulation layer. This renders claim 6 obvious. The inverter would include PMOS and NMOS transistors to closely correspond to the MOS transistors in Hardee's device, thus allowing all the transistors to be have similar fabrication processes and operating characteristics. The inverter transistors will have a thick oxide to prevent their breakdown, since they operate at the higher voltage VCCP (Vwl). Interpreting Hardee's Fig. 1 circuit in a slightly different manner, the device comprises a power terminal (i.e. the unlabeled connection between transistors 12 and 14) selectively receiving high voltage VCCP (Vwl) higher than power supply voltage VCC of the device; first transistor 12 having a drain coupled to the power terminal, a source coupled to high voltage VCCP (Vwl), a gate coupled to a first input signal that selectively alternates between 0V and VCCP (Vwl), and a thick gate insulation layer (i.e. THICK OXIDE); second transistor 14 having a drain coupled to the power terminal, a gate coupled to low voltage VCC lower than high voltage VCCP (Vwl), and a thin gate insulation layer (i.e. THIN OXIDE); and third transistor 16 having a drain coupled to the source of second transistor 14, a source coupled to a ground voltage, a gate coupled to a second input signal selectively alternating between 0V and VCC, and a thin gate insulation layer (i.e. THIN OXIDE). For the same type of reasoning as described above with respect to claim 1, the second input signal applied to the gate of third transistor 16 is capable of being, or with respect to Origasa can be, a row address signal

from a memory device. Therefore, claim 10 is rendered obvious. Since second voltage VCC is the power supply voltage, which is an external power supply voltage, or an internal power supply voltage, of the device, claim 11 is also rendered obvious. One of ordinary skill in the art would understand that 0V is a low level corresponding to the ground voltage. Therefore, the first input signal is selectable as one of a high level of high voltage VCCP (Vwl) and a low level of ground; and the second input signal is selectable as one of a high level of low voltage VCC and a low level of ground, rendering claims 12-13 obvious. Claims 15-16 are rendered obvious for the same reasoning as previously described above with claims 5-6, respectively. Hardee discloses that any number of NMOS transistor can be coupled in series to configure the switching circuit into a NAND logic configuration (e.g. see column 4, lines 29-36 and Fig. 4B). Therefore, it would have been obvious to one of ordinary skill in the art to couple a fourth transistor between third transistor 16 of Hardee and ground. This fourth transistor would have a thin gate insulation layer because it is related to the lower voltages within the device, not high voltage VCCP (Vwl). Therefore, claim 17 is rendered obvious. The fourth transistor would provide another means for dropping voltage, thus helping to distribute the total voltage drop between the power terminal (i.e. output terminal of the device) across more transistors. Also, if the fourth transistor is used as part of a NAND logic configuration, it is capable of receiving a block selecting signal from the memory device, rendering obvious claim 18. Configured as NAND logic, the device will provide a low output signal only when the second input signal, and the block selecting signal, allow the third and fourth transistors to conduct. This will help ensure that the device will generate a low only when these specific conditions are met, and only when a low output signal is actually desired. By re-identifying the restricting means of claim 1 as an interface circuit, claims

32-33 and 35 are rendered obvious for the same type of reasoning as previously described with respect to claims 1-2. Since third MOS transistor 14 functions as a resistance device, one of ordinary skill in the art would know that it prevents first voltage VCCP (Vwl) from being directly applied to the drain of second MOS transistor 16, thus enabling it to have the thin gate insulation layer, and reducing the gate-drain voltage of second MOS transistor 16 to alleviate the electric field applied to the gate insulation layer of second MOS transistor 16. This knowledge renders respective claims 36 and 37 obvious.

Claims 1-3, 5-6, 10-13, 15-16, 19-24, 26, 32-33, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Origasa, a reference found during the recent update search, and further in view of Wright et al. (Wright), reference D cited on the PTO-892 of paper number 02092006. Origasa shows a semiconductor integrated circuit device in Fig. 2 that is related to a memory device, wherein the device comprises word line driver 200, which is shown in detail in Fig. 3. In Fig. 3, driver 200 is shown comprising level shifter 30 comprising four MOS transistors 302-305 and inverter 306. However, each of the transistors comprises a thick gate insulation layer. Therefore, the reference does not show: 1) the third MOS transistor having a thin gate insulation layer as recited within claim 1; 2) the second/third transistors having a thin gate insulation layer as recited within claim 10; 3) the third-sixth MOS transistors with thin gate insulation layers as recited within claims 19-20; or 4) the second/third MOS transistors with thin gate insulation layers as recited within claim 32. Fig. 1 of Wright shows/discloses level shifter 100 that closely corresponds to level shifter 30 of Origasa, wherein all the transistors also have a thick oxide. However, Wright's Fig. 2 shows level shifter 200 that can replace Wright's Fig. 1 level shifter 100. Therefore, it would have been obvious to one of ordinary skill in the art to

replace level shifter 30 of Origasa with level shifter 200 of Wright. With this configuration, the device comprises first internal circuit 212, including first MOS transistor 212, operating at first voltage Vwl(VIO) higher than power supply voltage VCORE of the device (e.g. see column 1, lines 28-32 and 48-50); second internal circuit 204, including second MOS transistor 204, operating at second voltage VCORE (i.e. inverted VIN, on line 224, will have VCORE as its high logic level) lower than first voltage Vwl(VIO); and restricting means 208, including third MOS transistor 208 that can have a relatively thin gate insulation layer (e.g. see column 4, line 17-19, wherein a medium gate oxide is thinner than a thick gate oxide) and operating at second voltage VCORE, wherein one of ordinary skill in the art will know restricting means 208 will restrict a voltage transmitted from first internal circuit 212 to second internal circuit 204 by applying the voltage from first internal circuit 212 to second internal circuit 204 through third MOS transistor 208. Since second MOS transistor 204 is controlled by the inverted input signal VIN, which corresponds to the output of Origasa's logic gate 307, transistor 204 is effectively controlled by row address signal XAj,XBj. This renders claim 1 obvious. Since first MOS transistor 212 has a thick gate insulation layer (i.e. see column 4, lines 17-18), and second MOS transistor 204 has a thin gate insulation layer (i.e. see column 4, line 4), it would be obvious to one of ordinary skill in the art that the voltage transmitted from first internal circuit 212 to second internal circuit 204 would reduce an electric field applied to the gate insulation layer of second MOS transistor 204 since restricting means 208 functions at a resistance device that provides a voltage drop across it, thus rendering claim 2 obvious. Second voltage VCORE is a power supply voltage that is an internal power supply voltage for the device (e.g. see column 1, line 48-50), and claim 3 is rendered obvious. Connection node 220 of Wright, between first/third

MOS transistors 212/208, corresponds to line 308 of Origasa, which is coupled to inverter 300,301 that drives word line WL of the memory device, rendering claim 5 obvious. The inverter includes PMOS/NMOS transistors 300/301 operating at a third voltage Vwl(VIO) higher than power supply voltage VCORE when transistor 212 is conducting, wherein each transistor of the inverter has a thick gate insulation layer. This renders claim 6 obvious. Interpreting the Origasa/Wright configuration in a slightly different manner, the device comprises power terminal 308(220) selectively receiving high voltage Vwl(VIO) higher than power supply voltage VCORE; first transistor 212 having a drain coupled to the power terminal, a source coupled to high voltage Vwl(VIO), a gate coupled to a first input signal (from the common connection between 210 and 206), and a thick gate insulation layer (i.e. thick gate oxide); second transistor 208 having a drain coupled to the power terminal, a gate coupled to low voltage VCORE lower than high voltage Vwl(VIO), and a relatively thin gate insulation layer (i.e. a medium gate oxide is thinner than a thick gate oxide); and third transistor 204 having a drain coupled to the source of second transistor 208, a source coupled to a ground voltage, a gate coupled to a second input signal (i.e. an inverted version of Wright's input signal VIN, which corresponds to the output signal of Origasa's logic gate 307), and a thin gate insulation layer (i.e. thin gate oxide). For the same type of reasoning as described above with respect to claim 1, the second input signal applied to the gate of third transistor 204 effectively includes a row address signal from a memory device. Therefore, claim 10 is rendered obvious. Since second voltage VCORE is the power supply voltage that is an internal power supply voltage of the device, claim 11 is also rendered obvious. The first input signal, generated at the common connection between 210 and 206, is selectable as one of a high level of high voltage Vwl(VIO) when transistor 210 is

conducting, and a low level of ground when transistor 202 is conducting, thus rendering claim 12 obvious. The second input signal, provided at the output of Wright's inverter 214, is selectable as one of a high level of low voltage VCORE and a low level of ground, rendering claim 13 obvious. Claims 15-16 are rendered obvious for the same reasoning as previously described with respect to claims 5-6. In still another interpretation of the Origasa/Wright configuration, the device comprises power terminal 222 receiving high voltage Vwl(VIO) higher than power supply voltage VCORE of the device (e.g. see related column 1, lines 31-54); first MOS transistor 210 coupled between the power terminal and a first internal node (i.e. unlabeled connection between 210 and 206); second MOS transistor 212 coupled between the power terminal and second internal node 220; third MOS transistor 206 coupled between the first internal node and a third internal node (i.e. unlabeled connection between 206 and 202); fourth MOS transistor 208 coupled between second internal node 220 and a fourth internal node (i.e. unlabeled connection between 208 and 204); fifth MOS transistor 202 coupled between the third internal node and a ground voltage, and controlled by first input signal VIN; and sixth MOS transistor 204 coupled between the fourth internal node and the ground voltage, and controlled by an inverted version of first input signal VIN. The first input signal VIN effectively includes row address signal XAj,XBj and block selecting signal WDEN through logic gate 307. Wright discloses that first/second MOS transistors 210/212 have a relatively thick gate insulation layer (e.g. see "thick gate oxide" on column 4, lines 17-18); third/fourth MOS transistors 206/204 can have a relatively thin gate insulation layer (e.g. see "medium gate oxide" on column 4, lines 18-19); and fifth/sixth MOS transistors 202/204 have a relatively thin gate insulation layer (e.g. see "thin gate oxide" on column 4, line 4), thus rendering claims 19-20 obvious. The replacement of

Origasa's circuit 30 with Wright's circuit 200 replaces one level shifter with another level shifter. Improved level shifter 200 of Wright would allow the overall modified circuit of Origasa to operate at lower internal operating voltages, and faster speeds (e.g. see column 2, line 66 through column 3, line 14), and help prevent breakdown of the switching transistors due to the high voltage (e.g. see column 3, lines 15-24). Power supply voltage VCORE is an internal power supply voltage of the device (e.g. see column 1, lines 48-50), rendering claim 21 obvious. Since first MOS transistor 210 and second MOS transistor 212 are controlled by a voltage of the second and first internal nodes, respectively. Therefore claim 22 is rendered obvious. The gates of third/fourth MOS transistors 206/208 are each coupled to low voltage VCORE, which is lower than high voltage Vwl(VIO), and an internal power supply voltage of the device as previously described, thus rendering claims 23-24 obvious. With the positive and negative power supply terminals of inverter 214 connected to VCORE/ground, respectively, the first input signal and its inverted version are understood to be selectable, and will have one of a high level of low voltage VCORE and a low level of ground voltage, rendering obvious claim 26. By re-identifying the restricting means of claim 1 as an interface circuit, claims 32-33 and 35 are rendered obvious for the same type of reasoning as previously described with respect to claims 1-2. Since third MOS transistor 208 functions as a resistance device, one of ordinary skill in the art would know that it prevents first voltage Vwl(VIO) from being directly applied to the drain of second MOS transistor 204, thus enabling it to have the thin gate insulation layer, and reducing the gate-drain voltage of second MOS transistor 204 to alleviate the electric field applied to the gate insulation layer of second MOS transistor 204. This knowledge renders respective claims 36 and 37 obvious.

No claim is allowable as presently written.

Claims 4, 7-9, 14, 25, 27, and 34 have been cancelled.

Allowable Subject Matter

However, claims 28-31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is no presently no strong motivation to modify or combine any prior art reference(s) to ensure the first internal node of the Wright level shifter is coupled to a row decoder and driver block of the memory device, wherein that block selectively drives word lines of the memory device in response to row address signals. [For example, each of Origasa's drivers (i.e. see drivers 200 in Fig. 2) receives an input from row decoder 201 and provides an output going directly to a corresponding word line WL, wherein it is understood from the claims the output (understood to be at the first internal node) is supplied to the row decoder and driver block.]

Prior Art

The other reference cited on the accompanying PTO-892 is deemed relevant to the claimed invention for the same type of reasoning as described above. Although not used in any formal rejections described above, the reference of Wang et al. could have also been used in the same manner as Wright et al.'s reference, with respect to Origasa's reference. For example, Wang's Fig. 1 shows a level shifter P3-P4,N3-N4 that closely corresponds with Origasa's level shifter 30, and Wright et al.'s level shifter 100, wherein each transistor has a thick gate oxide (e.g. see column 1, lines 40-44; and how the gates are shown in the figure). Wang et al.'s Fig. 5 shows an improved level shifter 339,343,353 with MOS transistors P3-P4,ZN1-ZN2 having thick

oxides, and N3-N4,N6-N7 having thin oxides, wherein Wang et al. discloses the level shifter can be used with high speed and reliability, and also no static current (e.g. see column 3, lines 1-6). Wang et al. also discloses that transistors N6-N7 improve the high voltage reliability of the circuit for higher voltages (e.g. see column 7, lines 7-11).

Although not used in any formal rejections described above, reference E (i.e. by Chang et al.) cited on the PTO-892 of paper number 02092006, could have also been used in the same manner as Wright et al.'s reference, with respect to Origasa's reference. For example, Fig. 1(a) of Chang et al. shows level shifter 1 that closely corresponds with Origasa's level shifter 30, and Wright et al.'s level shifter 100, wherein each transistor has a thick gate oxide (e.g. see column 1, lines 38-42 of Chang et al.) Chang et al.'s Fig. 3 shows an improved level shifter 3 with MOS transistors PG1-PG2/NG1-NG2 having thick oxides, and N1-N4 having thin oxides (e.g. see column 3, lines 55-64). The Fig. 3 level shifter of Chang et al. is a high speed level shifter that can provide an output voltage with minimal distortion, even with a low input voltage (e.g. see column 2, lines 31-37).

Therefore, the references of Chang et al. and Wang et al. should be carefully reviewed and considered since one of ordinary skill in the art would know that one type of level shifter could be replaced with another level shifter (e.g. with respect to the Origasa reference).

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

9 January 2007

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